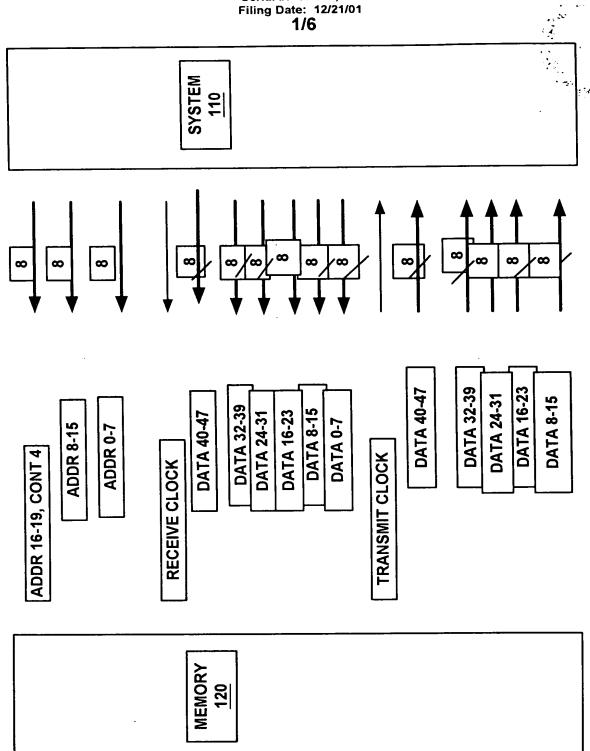
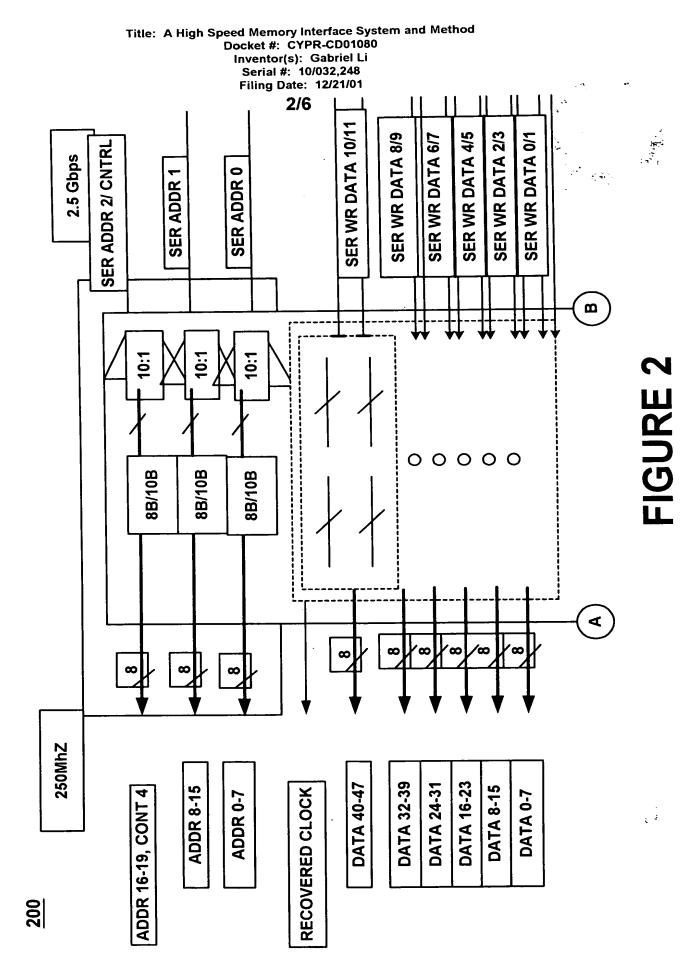


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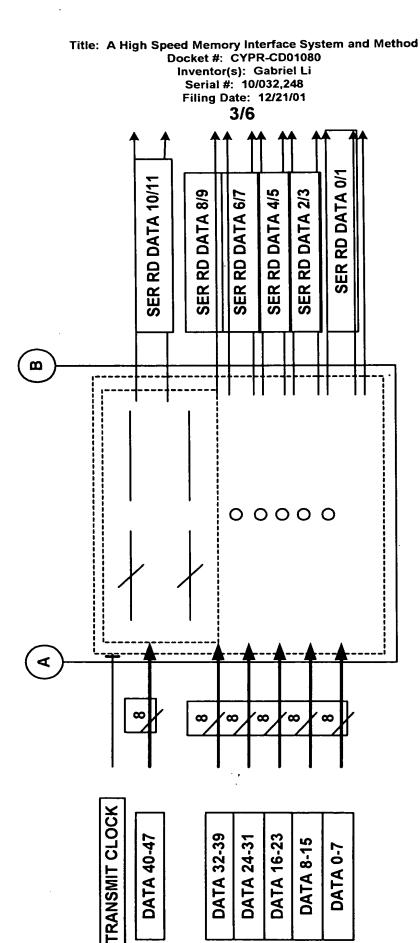


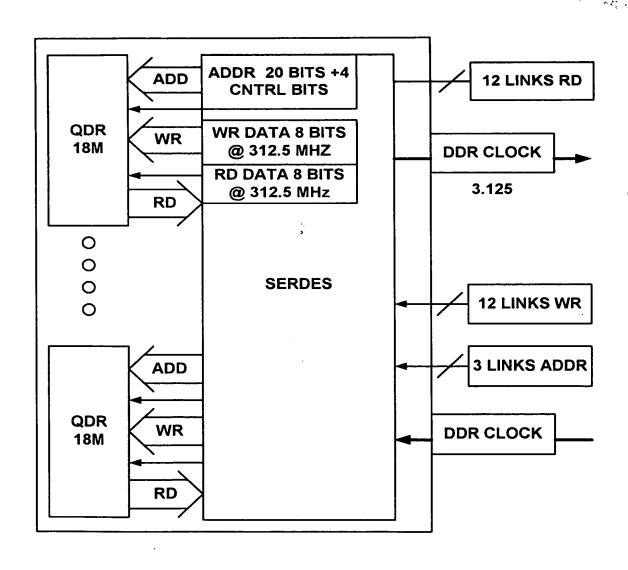
FIGURE 2 (CONT.)

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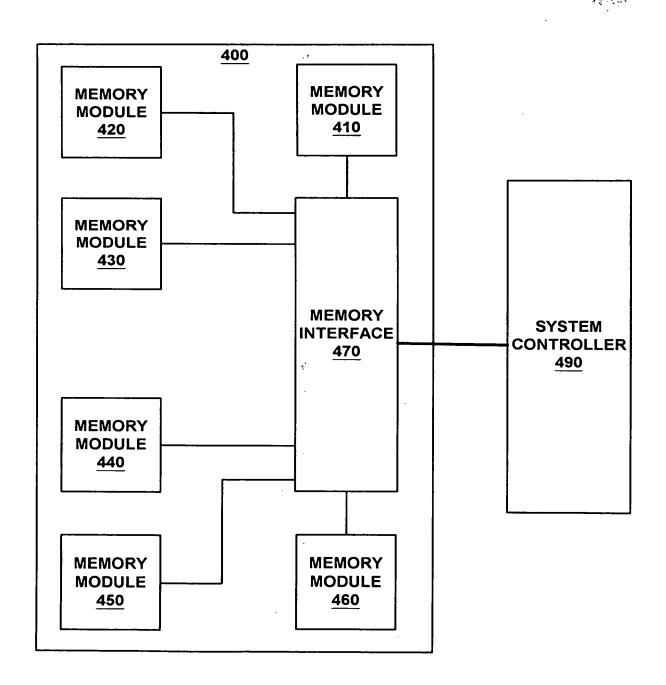
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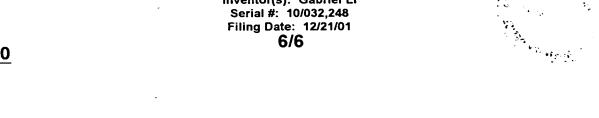
5/6

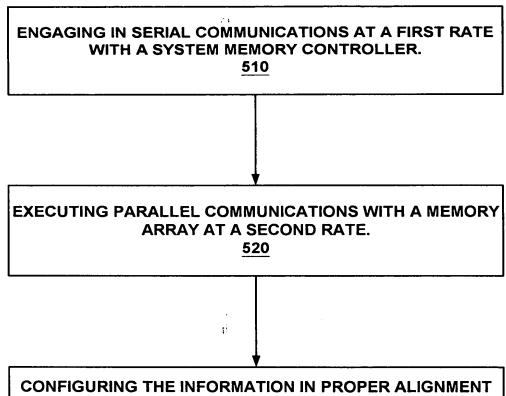


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FOR COMMUNICATION BETWEEN SERIAL SYSTEM CONTROLLER SIGNALS AND PARALLEL MEMORY ARRAY SIGNALS.

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